AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application.

LISTING OF CLAIMS

1. (currently amended) A bit synchronizing circuit used for a reception circuit for serial communication, comprising:

a polyphase clock generation circuit for generating a plurality of clocks which are out of phase with each other by a regular interval, based on an input clock; ~~and~~

a detection circuit for detecting which clock has a phase shift of an integral multiple of a clock cycle among the clocks generated by the polyphase clock generation circuit with respect to the input clock; and

a clock selecting circuit to which a polyphase is inputted from the polyphase clock generation circuit and which selects an outputted polyphase clock based on a detection result from the detection circuit.

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2. (original) The bit synchronizing circuit of claim 1, wherein the polyphase clock generation circuit is formed by connecting a plurality of

delay circuits which delay the input clock by almost the same amount of time.

3. (currently amended) A bit synchronizing circuit for a reception circuit for serial communication ~~The bit synchronizing circuit of claim 1~~, comprising:

a polyphase clock generation circuit for generating a plurality of clocks which are out of phase with each other by a regular interval, based on an input clock;

a detection circuit for detecting which clock has a phase shift of an integral multiple of a clock cycle among the clocks generated by the polyphase clock generation circuit with respect to the input clock;

a logic circuit to which an output from the detection circuit is inputted; and

a latch circuit to which an output from the logic circuit is inputted and of which an output is inputted to the logic circuit.

4. (original) The bit synchronizing circuit of claim 3, wherein the data of the latch circuit is cleared with a constant timing.

5. (currently amended) A bit synchronizing circuit used for a reception circuit for serial communication ~~The bit synchronizing circuit of claim 1~~, comprising:

a polyphase clock generation circuit for generating a plurality of clocks which are out of phase with each other by a regular interval, based on an input clock;

a detection circuit for detecting which clock has a phase shift of an integral multiple of a clock cycle among the clocks generated by the polyphase clock generation circuit with respect to the input clock; and

an operational circuit for sampling an output from the detection circuit a plurality of times and carrying out operations on sampled values.

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6. (currently amended) The bit synchronizing circuit of claim ~~1~~ 3, wherein an output from the detection circuit is held for a constant cycle time and is updated at each constant time unit.

7. (original) The bit synchronizing circuit of claim 6, wherein the output from the detection circuit is held at the time of bit data reception.

8. (currently amended) A bit synchronizing circuit used for a reception circuit for serial communication ~~The bit synchronizing circuit of claim 1~~, comprising:

a polyphase clock generation circuit for generating a plurality of clocks which are out of phase with each other by a regular interval, based on an input clock;

a detection circuit for detecting which clock has a phase shift of an integral multiple of a clock cycle among the clocks generated by the polyphase clock generation circuit with respect to the input clock;

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a plurality of bit synchronous working circuits to which a polyphase clock is inputted from the polyphase clock generation circuit so that a bit synchronizing operation is carried out at each different phase; and

a selecting circuit for selecting outputs from the plurality of bit synchronous working circuits, based on the detection result of the detection circuit.

9. (currently amended) The bit synchronizing circuit of claim ~~9~~ 3, comprising:

a clock selecting circuit to which a polyphase clock is inputted from the polyphase clock generation circuit and which selects an

outputted polyphase clock based on a detection result from the detection circuit.

10. (new) The bit synchronizing circuit of claim 5, wherein an output from the detection circuit is held for a constant cycle time and is updated at each constant time unit.

11. (new) The bit synchronizing circuit of claim 5, comprising:

a clock selecting circuit to which a polyphase clock is inputted from the polyphase clock generation circuit and which selects an outputted polyphase clock based on a detection result from the detection circuit.

12. (new) The bit synchronizing circuit of claim 3, wherein the polyphase clock generation circuit is formed by connecting a plurality of delay circuits which delay the input clock by almost the same amount of time.

13. (new) The bit synchronizing circuit of claim 5, wherein the polyphase clock generation circuit is formed by connecting a plurality of

delay circuits which delay the input clock by almost the same amount of time.

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14. (new) The bit synchronizing circuit of claim 8, wherein the polyphase clock generation circuit is formed by connecting a plurality of delay circuits which delay the input clock by almost the same amount of time.